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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/034,338	12/28/2001	Wayne A. Morgan	047711-0295	8387

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Irvin C. Harrington, III
FOLEY & LARDNER
2029 Century Park East, 35th Floor
Los Angeles, CA 90067-3021

EXAMINER


DOLE, TIMOTHY J

ART UNIT	PAPER NUMBER
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2858

DATE MAILED: 04/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/034,338	MORGAN ET AL.	
	Examiner	Art Unit	
	Timothy J. Dole	2858	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 21 November 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-3 and 5-38 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-3, 5-25 and 27-31 is/are rejected.
- 7) ☒ Claim(s) 26 and 32-38 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-3, 5, 23-25, 27, 28 and 30 are rejected under 35 U.S.C. 102(b) as being anticipated by Otagawa et al.

Regarding claim 1, Otagawa et al. discloses an electronic circuit for sensing an output of a sensor, the electronic circuit comprising: a substrate (fig. 11 (12)); at least two electrode pairs (fig. 3 (10)) formed on the surface of the substrate (fig. 11) for sensing a parameter, each electrode pair having a first electrode (fig. 11 (30)) and a second electrode (fig. 11 (18)), wherein the first electrode of each electrode pair wraps at least partially around the second electrode of its electrode pair (fig. 1); and circuitry for processing the parameter (column 15, lines 24-31), wherein a layout of the first electrode and the second electrode minimizes cross coupling between the first electrode and the second electrode. It should be noted that since the first electrode partially wraps around the second electrode as shown in fig. 11, cross coupling between the first and second electrode would inevitably be minimized.

Regarding claim 2, Otagawa et al. discloses the circuit as claimed wherein the first electrode of each electrode pair (fig. 11 (30)) wraps around the second electrode of its electrode pair (fig. 11 (18)) in a U-shaped fashion (fig. 11).

Regarding claim 3, Otagawa et al. discloses the circuit as claimed wherein the first electrode of each electrode pair (fig. 11 (30)) wraps around the second electrode of its electrode pair (fig. 11 (18)) by surrounding three sides of the second electrode (fig. 11).

Regarding claim 5, Otagawa et al. discloses the circuit as claimed, further comprising a reference electrode for setting a reference voltage for the at least two electrode pairs (fig. 11 (32)).

Regarding claim 23, Otagawa et al. discloses the circuit as claimed wherein at least one of the first electrode and the second electrode is electroplated (column 7, lines 20-30).

Regarding claim 24, Otagawa et al. discloses the circuit as claimed wherein the first electrode is coplanar with the second electrode (fig. 11).

Regarding claim 25, Otagawa et al. discloses the circuit as claimed wherein the first electrodes of the at least two electrode pairs are electronically coupled to each other (column 6, lines 60-68).

Regarding claim 27, Otagawa et al. discloses the circuit as claimed, further comprising a spacer covering the at least two electrode pairs (fig. 2 (42)).

Regarding claim 28, Otagawa et al. discloses the circuit as claimed wherein the spacer includes an area for containing a biomolecule such that the biomolecule is located adjacent to at least one of the at least two electrode pairs (column 6, lines 37-59).

Referring to claim 30, Otagawa et al. discloses the circuit as claimed wherein the spacer comprises a material that is permeable to oxygen and is not permeable to the biomolecule (column 6, lines 37-59).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 6 and 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Otagawa et al., in view of Schulman et al.

Regarding claim 6, Otagawa et al. does not disclose the reference voltage set on the reference electrode is 0.5 volts.

Schulman et al. discloses an electronic circuit for sensing the output of a sensor (fig. (10)), wherein the electronic circuit comprises a reference electrode (fig. 6 (REF1)) for setting a reference voltage and that the reference voltage is about 0.5 volts (column 7, line 17; and column 12, lines 20-21).

At the time of the invention, it would be obvious to a person of ordinary skill in the art to combine the teaching of Schulman et al. into Otagawa et al. for the purpose of

setting a known reference voltage against which the voltages measured by the at least two electrode pairs can be assessed.

Regarding claims 20-22, which depend on claim 1, Otagawa et al. does not disclose that the parameter sensed by the at least two electrode pairs is a physiological parameter and the said physiological parameter is glucose or oxygen.

Schulman et al. discloses an implantable sensor (title; abstract; and; column 1, line 8) that senses glucose (column 2, line 16) and oxygen (column 5, lines 1-2).

At the time of the invention, it would be obvious to a person of ordinary skill in the art to combine the teaching of Schulman et al. into Otagawa et al. for the purpose of monitoring a patient's blood or other body-fluid characteristics (Schulman et al., column 1, lines 20-22).

5. Claims 7, 8, 10, 13 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Otagawa et al., in view of Preikschat.

Regarding claim 7, Otagawa et al. discloses the circuit as claimed except wherein the circuitry comprises a line interface for interfacing with input/output lines, a rectifier in parallel with the line interface, a counter connected to the line interface, and a data converter connected to the counter and the at least two electrode pairs.

Preikschat discloses electrode arrangements (fig. 1 (12), column 4, lines 28-34; fig. 4 (100), column 6, lines 65-66; and fig. 7 (152) and (154), column 10, lines 1 ff) and associated circuitry (fig. 1) for measuring the electrical properties of various materials (abstract; column 1, lines 18-23) comprising: a line interface (fig. 1 (44)) for interfacing with input/output lines (fig. 1 (46)), a rectifier (fig. 1 (44), column 4, lines 44-46) in

parallel with the line interface (fig. 1 (44), column 4, line 55; and fig. 6 (144), column 8, line 55 and column 9, line 31), a counter (fig. 12 (216) or (210); and column 16, line 13) connected to the line interface (fig. 12; through decoders (211) and (212), which receive inputs from the bridge circuits in fig. 1), and a data converter (fig. 1 (56)) connected to the counter (through the decoders, fig. 12 (211) and (212)) and the at least two electrode pairs (fig. 1 Es in (12), (32), (34), (36) and (38), column 4, lines 28-34).

At the time of the invention, it would be obvious to a person of ordinary skill in the art to combine the teaching of Preikschat into Otagawa et al. for the purpose making accurate measurements of sensed parameters.

Regarding claim 8, Otagawa et al. discloses the circuit as claimed except for further comprising control logic connected to the counter and the line interface.

Preikschat discloses control logic (fig. 12; and column 16, lines 2) connected to the counter (fig. 12 (210) or (216)) and the line interface (through decoders (211) and (212) and the bridge circuits).

At the time of the invention, it would be obvious to a person of ordinary skill in the art to combine the teaching of Preikschat into Otagawa et al. and incorporate a counter and control logic in the circuit, for the purpose of timing and controlling the measurements (Preikschat, column 11, lines 60 ff).

Regarding claim 10, Otagawa et al. discloses the circuit as claimed except wherein the control logic comprises a microprocessor.

Preikschat discloses that the control logic uses a microprocessor (fig. 6; and column 8, line 64).

At the time of the invention, it would be obvious to a person of ordinary skill in the art to combine the teaching of Preikschat into Otagawa et al. and incorporate a microprocessor in the circuit, for the purpose of automatic control of the sensing and for processing of the data sensed.

Regarding claim 13, Otagawa et al. discloses the circuit as claimed except wherein the data converter is and analog-to-digital converter.

Preikschat discloses that the data converter is an analog-to-digital converter (figs. 1 and 6 (56)).

At the time of the invention, it would be obvious to a person of ordinary skill in the art to combine the teaching of Preikschat into Otagawa et al. and incorporate an analog-to-digital converter in the circuit, for the purpose of further processing the data in a digital device such as a microcomputer.

Regarding claim 19, Otagawa et al. discloses the circuit as claimed except for switched capacitor circuits for use as resistors in the electronic circuit.

Preikschat discloses using switched capacitor (fig. 2 (62) and (86)) circuits as resistors (fig. 2; and column 5, lines 3-20).

At the time of the invention, it would be obvious to a person of ordinary skill in the art to combine the teaching of Preikschat into Otagawa et al. and incorporate switched capacitors as resistors in the circuit for the purpose of sensitive control of bridge circuits for measuring small electrode voltages.

6. Claim 9 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Otagawa et al. and Preikschat, as applied to claims 7 and 8 above, and further in view of Schulman et al.

Regarding claim 9, Otagawa et al. as modified discloses the circuit as claimed except wherein the control logic a state machine; and a state decoder connected to the state machine.

Schulman et al. discloses an electronic circuitry (abstract; and fig. 6) for sensing the output of a sensor (fig. 5 (10)), wherein the control logic (fig. 6) comprises a state machine (fig. 6 (138) and column 10, line 41) and a state decoder (fig. 6 (140)) connected to the state machine.

At the time of the invention, it would be obvious to a person of ordinary skill in the art to combine the teaching of Schulman et al. into the circuit of Otagawa et al. as modified and incorporate a state machine and a state decoder, for the purpose of ease of control of the tests by external command signals (Schulman et al., column 10, lines 40-44).

Regarding claim 18, Otagawa et al. as modified discloses the circuit as claimed except for a temperature sensor for reading a temperature of the environment and a voltage reference for applying a voltage to the reference electrode.

Preikschat discloses a temperature sensor (fig. 1 (20)) for reading the temperature of the environment (column 2, lines 56-58; and column 6, lines 40-43).

Schulman et al. discloses a voltage reference for applying a voltage to the reference electrode (column 12, lines 20-22).

At the time of the invention, it would be obvious to a person of ordinary skill in the art to combine the teaching of Schulman et al. into the circuit of Otagawa et al. and

Art Unit: 2858

Preikschat for the purpose of temperature compensation of any reading referenced to the reference voltage.

7. Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Otagawa et al. and Preikschat, as applied to claim 7 above, and further in view of Jones.

Regarding claims 11 and 12, Otagawa et al. as modified discloses the circuit as claimed except wherein the rectifier transfers power from communication pulses to a capacitor, and wherein the capacitor powers the electronic circuit using power stored from the communication pulses.

Jones discloses a compact power supply (title; and abstract), wherein a rectifier (fig. 1 (11)) transfers power from communication pulses (fig. 1 (15)) to a capacitor (fig. 2 (13')), and wherein the capacitor powers the electronic circuit (column 1, lines 14-16) using power stored from the communication pulses (fig. 1).

At the time of the invention, it would be obvious to a person of ordinary skill in the art to combine the teaching of Jones into the circuit of Otagawa et al. as modified for the purpose of supplying electrical power to the circuit.

8. Claims 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Otagawa et al., in view of Preikschat, as applied to claim 7 above, and further in view of Gord et al.

Regarding claims 14-15, Otagawa et al. as modified discloses the circuit as claimed except wherein the electronic circuit includes a data converter that is a voltage-to-frequency converter or a current-to-frequency converter.

Gord et al. discloses an electronic circuitry (abstract; and figs. 5A, 5B and 5C) for sensing the output of a sensor (figs. 1 and 2), wherein the output data is converted to

Art Unit: 2858

frequency (column 11, lines 28 ff) by a data converter that is an voltage-to frequency converter (column 11, line 31) or a current-to-frequency converter (fig. 5A (70); and column 11, lines 39-40).

At the time of the invention, it would be obvious to a person of ordinary skill in the art to combine the teaching of Gord et al. into the circuit of Otagawa et al. as modified for the purpose of sensing the output data, as a pulse train, with a counter (Gord et al., column 11 lines 48-51).

9. Claims 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Otagawa et al., Preikschat and Gord et al., as applied to claim 15 above, and further in view of Niezgoda et al.

Regarding claims 16-17, Otagawa et al. as modified discloses the circuit as claimed except wherein an output of the current-to-frequency converter is scaled using a prescaler before connecting to the counter and that the prescaler is a divide-by-16 prescaler.

Niezgoda et al. discloses a digital tone (frequency) processing circuit (title; and abstract), wherein the input to a counter is scaled using a prescaler before connecting to the counter (figs. 1, 2, 5, 9 and 10) and that the prescaler is a divide-by-16 prescaler (fig. 9; and column 12, line 18).

At the time of the invention, it would be obvious to a person of ordinary skill in the art to combine the teaching of Gord et al. into the circuit of Otagawa et al. as modified for the purpose of adjusting the (digital) signals to the capabilities of the counter.

Art Unit: 2858

10. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Otagawa et al. in view of Shiraki et al.

Otagawa et al. discloses the circuit as claimed except wherein the biomolecule is a glucose oxidase enzyme.

Shiraki et al. discloses a circuit (fig. 14) for sensing the output of a sensor (fig. 13) wherein the biomolecule is a glucose oxidase enzyme (page 7, paragraph 109).

At the time of the invention, it would be obvious to a person of ordinary skill in the art to combine the teaching of Shiraki et al. into the circuit of Otagawa et al. for the purpose of detecting specific contents of blood.

11. Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Otagawa et al. in view of Kespohl.

Otagawa et al. discloses the circuit as claimed wherein the first electrodes of each pair have a U-shape including an open end (fig. 11), the at least two electrode pairs being formed on the first surface of the substrate (fig. 3).

Otagawa et al. does not disclose that the open ends face in opposing directions.

Kespohl discloses a circuit (fig. 5) for sensing the output of a sensor (fig. 6) wherein the electrodes (fig. 5 (2-5)) are configured such that the first electrodes (fig. 5 (2) and (4)) of each pair have a U-shape including an open end, such that the open ends face in opposing directions (fig. 5).

At the time of the invention, it would be obvious to a person of ordinary skill in the art to combine the teaching of Kespohl into the circuit of Otagawa et al. for the purpose of obtaining an accurate signal that is free of interferences.

Allowable Subject Matter

1. Claims 26, and 32-38 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

2. Applicant's arguments filed November 21, 2003 have been fully considered but they are not persuasive.

3. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., "the reference electrode is disposed in between each electrode pair, separating the electrode pairs" and "the first electrode separates the reference electrode and the second electrode", page 8, first lines of second and third paragraphs, respectively) are not recited in rejected Claim 1. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Timothy J. Dole whose telephone number is (571) 272-2229.

The examiner can normally be reached on Mon. thru Fri. from 8:00 to 4:30.

Art Unit: 2858

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, N. Le can be reached on (571) 272-2233. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TJD

TJA J. DL



N. Le
Supervisory Patent Examiner
Technology Center 2800